REMARKS

The specification has been amended to correct minor obvious errors. A marked up version of the amended paragraphs of the specification is attached hereto pursuant to 37 C.F.R. § 1.121(b)(iii). Claims 1, 14 and 15 have been amended for clarity. A marked up version of the amended claims is also attached hereto pursuant to 37 C.F.R. § 1.121(c)(ii). New claims 16-23 have been added. Claims 2-13 remain unchanged. Thus, claims 1-23 are presently pending in this application for consideration.

The amendments to the present application are made to place the application in better form and to place the application in condition for allowance. No new matter has been added. Entry and consideration of these amendments prior to the first Office Action are respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at Los Angeles, California, telephone number (213) 337-6742 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,

HOGAN & HARTSON L.L.P.

Date: July 25, 2002

By: _____

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Version with markings to show changes made:

IN THE SPECIFICATION:

Please amend the paragraph starting on page 1, line 27 through page 3, line 6 as follows:

A semiconductor device according to a first aspect of the present invention [is provided with a memory cell including a first driver transistor, a second driver transistor, a first transfer transistor, a second transfer transistor, a first load transistor and a second load transistor, the semiconductor device comprises:] includes a first gate-gate electrode layer including a gate electrode of [the] a first load transistor and a gate electrode of [the] a first driver transistor[;] and a second gate-gate electrode layer including a gate electrode of [the] a second load transistor and a gate electrode of [the] a second driver transistor[;]. The semiconductor device also includes a first drain-drain wiring layer which forms a part of a connection layer that electrically connects a drain region of the first load transistor and a drain region of the first driver transistor[;] and a second drain-drain wiring layer which forms a part of a connection layer that electrically connects a drain region of the second load transistor and a drain region of the second driver transistor[;]. The semiconductor device further includes a first drain-gate wiring layer which forms a part of a connection layer that electrically connects the first gate-gate electrode layer and the second drain-drain wiring layer[;] and a second drain-gate wiring layer which forms a part of a connection layer that electrically connects the second gate-gate electrode layer and the first drain-drain wiring layer, wherein the first drain-gate wiring layer and the second drain-gate wiring layer are located in different layers, respectively, and wherein a width of the first gate-gate electrode layer in the first load transistor is larger than the width of the first gate-gate electrode layer in the first driver transistor.

Please delete the paragraphs starting on page 3, line 7 through page 6, line 27 as follows:

[The "wiring layer" means a conductive layer disposed over a field or an interlayer dielectric layer.

In accordance with this aspect of the present invention, the second drain-gate wiring layer is located in a layer over the first drain-gate wiring layer. In other words, the first drain-gate wiring layer and the second drain-gate wiring layer are located in different layers, respectively. As a result, the pattern density of a wiring layer in each of the layers where the first drain-gate wiring layer and the second drain-gate wiring layer are formed, respectively, can be reduced and the cell area may be smaller compared to the case where the first drain-gate wiring layer and the second drain-gate wiring layer are formed in the same layer.

The width of the first gate-gate electrode layer in the first load transistor is larger than the width of the first gate-gate electrode layer in the first driver transistor. As a result, for the reasons described below, leak current in the first load transistor can be decreased.

The semiconductor device of this aspect may take at least any one of the following features.

(a) A width of the second gate-gate electrode layer in the second load transistor may be larger than the width of the second gate-gate electrode layer in the second driver transistor. In this feature, leak current in the second load transistor can be decreased for the reasons described below.

(b) The semiconductor device may comprise a first adjacent memory cell which is located adjacent to a side of the memory cell where the first gate-gate electrode layer is provided,

the first adjacent memory cell may include a third gate-gate electrode layer having a gate electrode of a third load transistor and a gate electrode of a third driver transistor,

the first load transistor and the third load transistor commonly may use a first impurity layer as a source region,

a first contact section may be provided on the first impurity layer, and

the first contact section may be provided in a region other than a region between the first gate-gate electrode layer and the third gate-gate electrode layer.

In this feature, a sufficient space between the first or third gate-gate electrode layer and the first contact section can be secured, so that short circuit between them can be decreased.

(c) The semiconductor device may comprise a second adjacent memory cell which is located adjacent to a side of the memory cell where the second gate-gate electrode layer is provided,

the second adjacent memory cell may include a fourth gate-gate electrode layer having a gate electrode of a fourth load transistor and a gate electrode of a fourth driver transistor,

the second load transistor and the fourth load transistor may commonly use a second impurity layer as a source region,

a second contact section may be provided on the second impurity layer, and

the second contact section may be provided in a region other than a region between the second gate-gate electrode layer and the fourth gate-gate electrode.

In this feature, a sufficient space between the second or fourth gate-gate electrode layer and the second contact section can be secured, such that short circuit between them can be decreased.

(d) The first drain-gate wiring layer may be electrically connected to the second drain-drain wiring layer through a contact section, and

the second drain-gate wiring layer may be electrically connected to the second gate-gate electrode layer through a contact section, and electrically connected to the first drain-drain wiring layer through a contact section.

(e) The first drain-gate wiring layer may be located in a layer lower than the second drain-gate wiring layer.

(f) The first drain-gate wiring layer may be located in a layer in which the first gate-gate electrode layer is provided.

(g) The second drain-gate wiring layer may be formed across a plurality of layers.

In the feature of (g), the second drain-gate wiring layer may include a lower layer of the second drain-gate wiring layer and an upper layer of the second drain-gate wiring layer, and

the upper layer may be located in a layer over the lower layer, and electrically connected to the lower layer.

Further, in this feature, the upper layer may be electrically connected to the lower layer through a contact section.

Further, in this feature, the first gate-gate electrode layer, the second gate-gate electrode layer and the first drain-gate wiring layer may be located in a first conductive layer,

the first drain-drain wiring layer, the second drain-drain wiring layer and the lower layer may be located in a second conductive layer, and

the upper layer may be located in a third conductive layer.

(h) The second conductive layer may be a nitride layer of a refractory metal (for example, titanium nitride). As a result of the second conductive layer being a nitride layer of a refractory metal, the thickness of the second conductive layer can be reduced, and miniaturizing processing can be readily performed. Accordingly, the cell area may be reduced. The second conductive layer may have a thickness of 100 nm to 200 nm.]

Please insert the following paragraphs starting on page 9, line 14.

A semiconductor device according to a first aspect of the present invention includes a first gate-gate electrode layer including a gate electrode of a first load transistor and a gate electrode of a first driver transistor and a second gate-gate electrode layer including a gate electrode of a second load transistor and a gate electrode of a second driver transistor. The semiconductor device also includes a first drain-drain wiring layer which forms a part of a connection layer that electrically connects a drain region of the first load transistor and a drain region of the first driver transistor and a second drain-drain wiring layer which forms a part of a connection layer that electrically connects a drain region of the second load transistor and a drain region of the second driver transistor. The semiconductor device further includes a first drain-gate wiring layer which forms a part of a connection layer that electrically connects the first gate-gate electrode layer and the second drain-drain wiring layer and a second drain-gate wiring layer which forms a part of a connection layer that electrically connects the second gate-gate electrode layer and the first drain-drain wiring layer, wherein the first drain-gate wiring layer and the second drain-gate wiring layer are located in different layers, respectively, and wherein a width of the first gate-gate

electrode layer in the first load transistor is larger than the width of the first gate-gate electrode layer in the first driver transistor.

The "wiring layer" means a conductive layer disposed over a field or an interlayer dielectric layer.

In accordance with this aspect of the present invention, the second drain-gate wiring layer is located in a layer over the first drain-gate wiring layer. In other words, the first drain-gate wiring layer and the second drain-gate wiring layer are located in different layers, respectively. As a result, the pattern density of a wiring layer in each of the layers where the first drain-gate wiring layer and the second drain-gate wiring layer are formed, respectively, can be reduced and the cell area may be smaller compared to the case where the first drain-gate wiring layer and the second drain-gate wiring layer are formed in the same layer.

The width of the first gate-gate electrode layer in the first load transistor is larger than the width of the first gate-gate electrode layer in the first driver transistor. As a result, for the reasons described below, leak current in the first load transistor can be decreased.

The semiconductor device of this aspect may take at least any one of the following features.

(a) A width of the second gate-gate electrode layer in the second load transistor may be larger than the width of the second gate-gate electrode layer in the second driver transistor. In this feature, leak current in the second load transistor can be decreased for the reasons described below.

(b) The semiconductor device may comprise a first adjacent memory cell which is located adjacent to a side of the memory cell where the first gate-gate electrode layer is provided, the first adjacent memory cell may include a third gate-gate electrode layer having a gate electrode of a third load transistor and a gate electrode of a third driver transistor, the first load

transistor and the third load transistor commonly may use a first impurity layer as a source region, a first contact section may be provided on the first impurity layer, and the first contact section may be provided in a region other than a region between the first gate-gate electrode layer and the third gate-gate electrode layer.

In this feature, a sufficient space between the first or third gate-gate electrode layer and the first contact section can be secured, so that short circuit between them can be decreased.

(c) The semiconductor device may comprise a second adjacent memory cell which is located adjacent to a side of the memory cell where the second gate-gate electrode layer is provided, the second adjacent memory cell may include a fourth gate-gate electrode layer having a gate electrode of a fourth load transistor and a gate electrode of a fourth driver transistor, the second load transistor and the fourth load transistor may commonly use a second impurity layer as a source region, a second contact section may be provided on the second impurity layer, and the second contact section may be provided in a region other than a region between the second gate-gate electrode layer and the fourth gate-gate electrode.

In this feature, a sufficient space between the second or fourth gate-gate electrode layer and the second contact section can be secured, such that short circuit between them can be decreased.

(d) The first drain-gate wiring layer may be electrically connected to the second drain-drain wiring layer through a contact section, and the second drain-gate wiring layer may be electrically connected to the second gate-gate electrode layer through a contact section, and electrically connected to the first drain-drain wiring layer through a contact section.

(e) The first drain-gate wiring layer may be located in a layer lower than the second drain-gate wiring layer.

(f) The first drain-gate wiring layer may be located in a layer in which the first gate-gate electrode layer is provided.

(g) The second drain-gate wiring layer may be formed across a plurality of layers.

In the feature of (g), the second drain-gate wiring layer may include a lower layer of the second drain-gate wiring layer and an upper layer of the second drain-gate wiring layer, and the upper layer may be located in a layer over the lower layer, and electrically connected to the lower layer.

Further, in this feature, the upper layer may be electrically connected to the lower layer through a contact section.

Further, in this feature, the first gate-gate electrode layer, the second gate-gate electrode layer and the first drain-gate wiring layer may be located in a first conductive layer, the first drain-drain wiring layer, the second drain-drain wiring layer and the lower layer may be located in a second conductive layer, and the upper layer may be located in a third conductive layer.

(h) The second conductive layer may be a nitride layer of a refractory metal (for example, titanium nitride). As a result of the second conductive layer being a nitride layer of a refractory metal, the thickness of the second conductive layer can be reduced, and miniaturizing processing can be readily performed. Accordingly, the cell area may be reduced. The second conductive layer may have a thickness of 100 nm to 200 nm.

IN THE ABSTRACT:

Please amend the original Abstract of the Disclosure as indicated below.

A semiconductor device is provided with [an SRAM] a memory cell. The semiconductor device includes a first gate-gate electrode layer, a second

gate-gate electrode layer, a first drain-drain wiring layer, a second drain-drain wiring layer, a first drain-gate wiring layer and second drain-gate wiring layers. The first drain-gate wiring layer and an upper layer and a lower layer of the second drain-gate wiring layer are located in different layers, respectively. The width of the first gate-gate electrode layer in the first load transistor is larger than the width of the first gate-gate electrode layer in the first driver transistor.

IN THE CLAIMS:

Please amend the claims as indicated below:

1. (Once Amended) A semiconductor device [provided with a memory cell including a first driver transistor, a second driver transistor, a first transfer transistor, a second transfer transistor, a first load transistor and a second load transistor, the semiconductor device] comprising:

a first gate-gate electrode layer including a gate electrode of [the] a first load transistor and a gate electrode of [the] a first driver transistor;

a second gate-gate electrode layer including a gate electrode of [the] a second load transistor and a gate electrode of [the] a second driver transistor;

a first drain-drain wiring layer which forms a part of a connection layer that electrically connects a drain region of the first load transistor and a drain region of the first driver transistor;

a second drain-drain wiring layer which forms a part of a connection layer that electrically connects a drain region of the second load transistor and a drain region of the second driver transistor;

a first drain-gate wiring layer which forms a part of a connection layer that electrically connects the first gate-gate electrode layer and the second drain-drain wiring layer; and

a second drain-gate wiring layer which forms a part of a connection layer that electrically connects the second gate-gate electrode layer and the first drain-drain wiring layer,

wherein the first drain-gate wiring layer and the second drain-gate wiring layer are located in different layers, respectively, and

wherein a width of the first gate-gate electrode layer in the first load transistor is larger than the width of the first gate-gate electrode layer in the first driver transistor.

14. (Once Amended) A memory system provided with the semiconductor device defined in [any one of claims] claim 1 [to 13].

15. (Once Amended) An electronic apparatus provided with the semiconductor device defined in [any one of claims] claim 1 [to 13].

ABSTRACT OF THE DISCLOSURE

A semiconductor device is provided with a memory cell. The semiconductor device includes a first gate-gate electrode layer, a second gate-gate electrode layer, a first drain-drain wiring layer, a second drain-drain wiring layer, a first drain-gate wiring layer and second drain-gate wiring layers. The first drain-gate wiring layer and an upper layer and a lower layer of the second drain-gate wiring layer are located in different layers, respectively. The width of the first gate-gate electrode layer in the first load transistor is larger than the width of the first gate-gate electrode layer in the first driver transistor